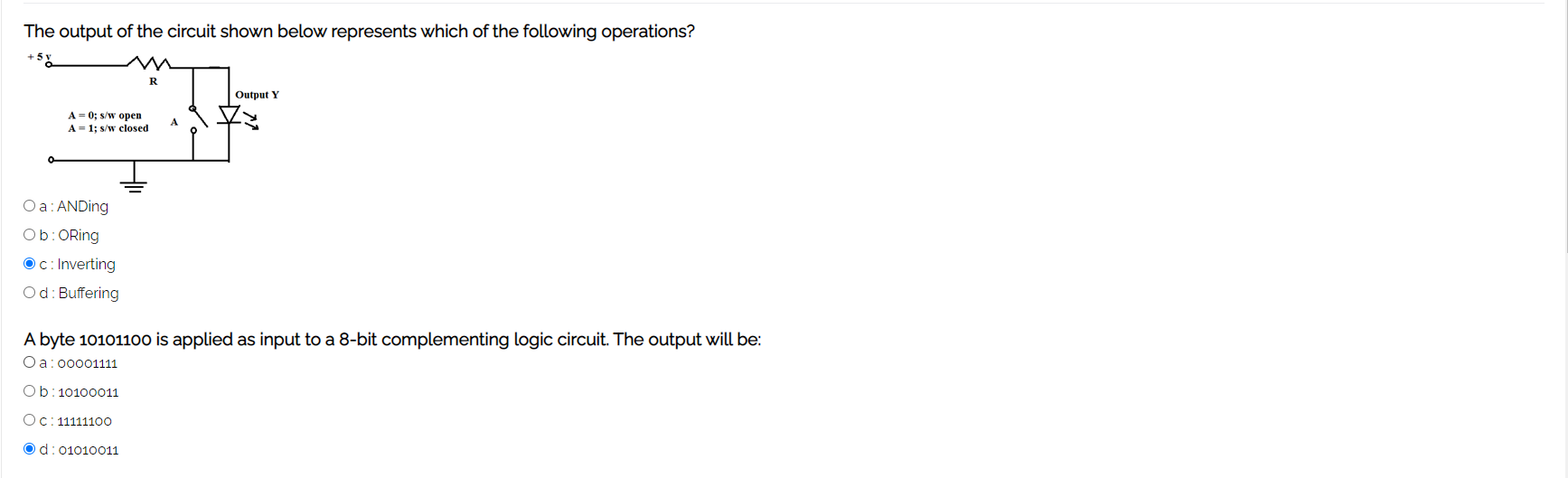
|  |  |
| --- | --- |
| **Name :-** | Aryan Dilipbhai Langhanoja |
| **Enroll No: -** | 92200133030 |

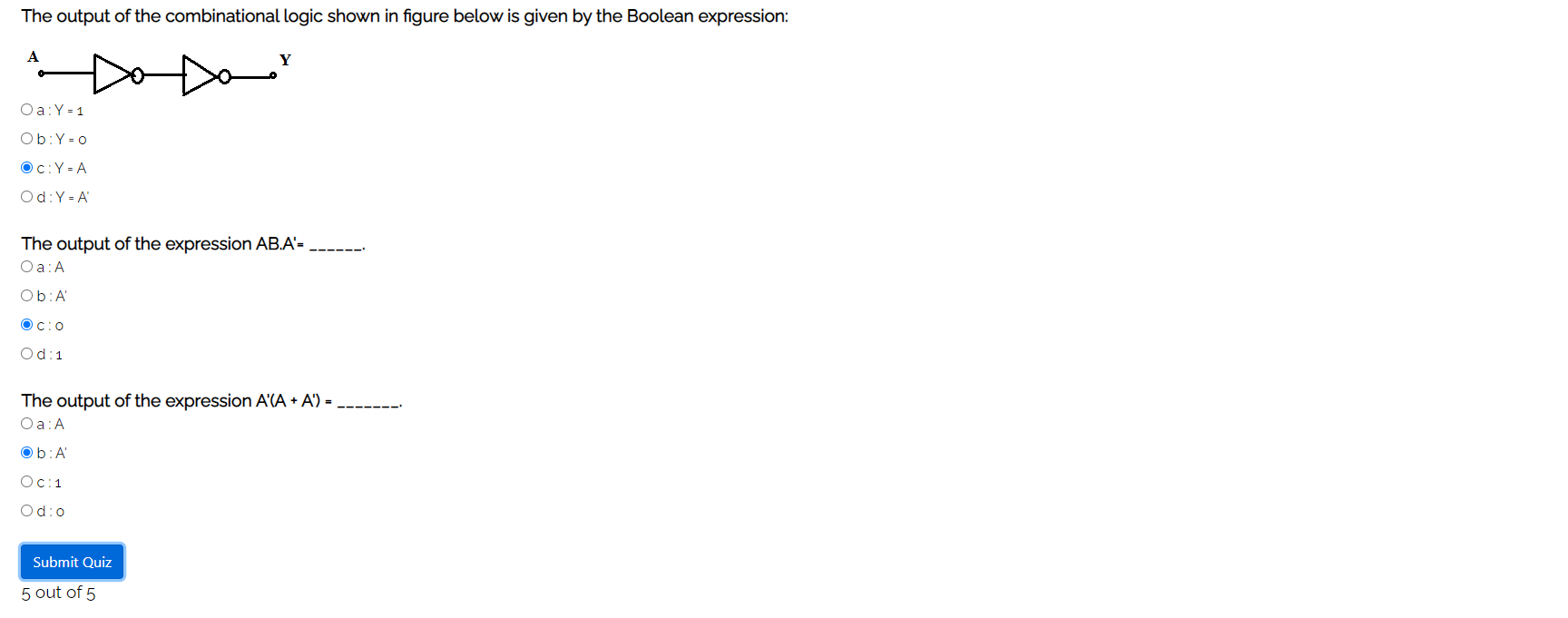
## Basics of NOT gate and its application in an 8-bit one's complement circuit

* **Aim** :-

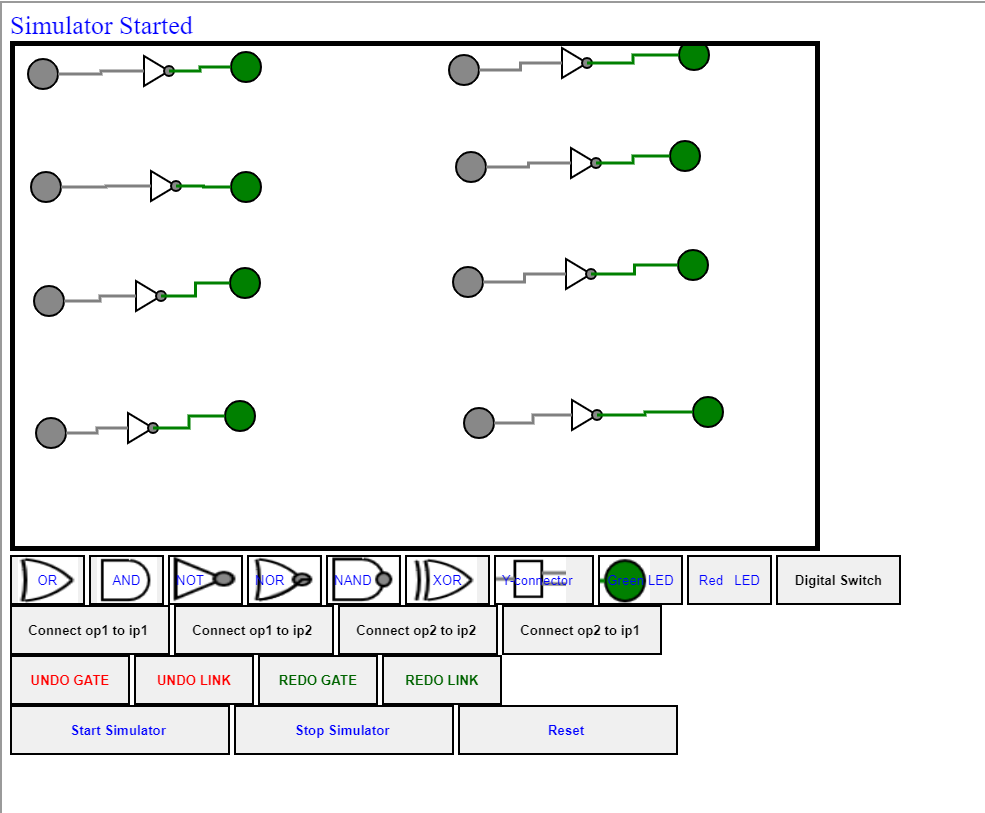
The aim of this experiment is to apply a basic NOT gate logic in a 8 -bit one’s complement circuit. The user will be able to build, simulate and verify the 8-bit one’s complementing circuit using the generalized simulator (a blank canvas with click & place facility for selected gates).

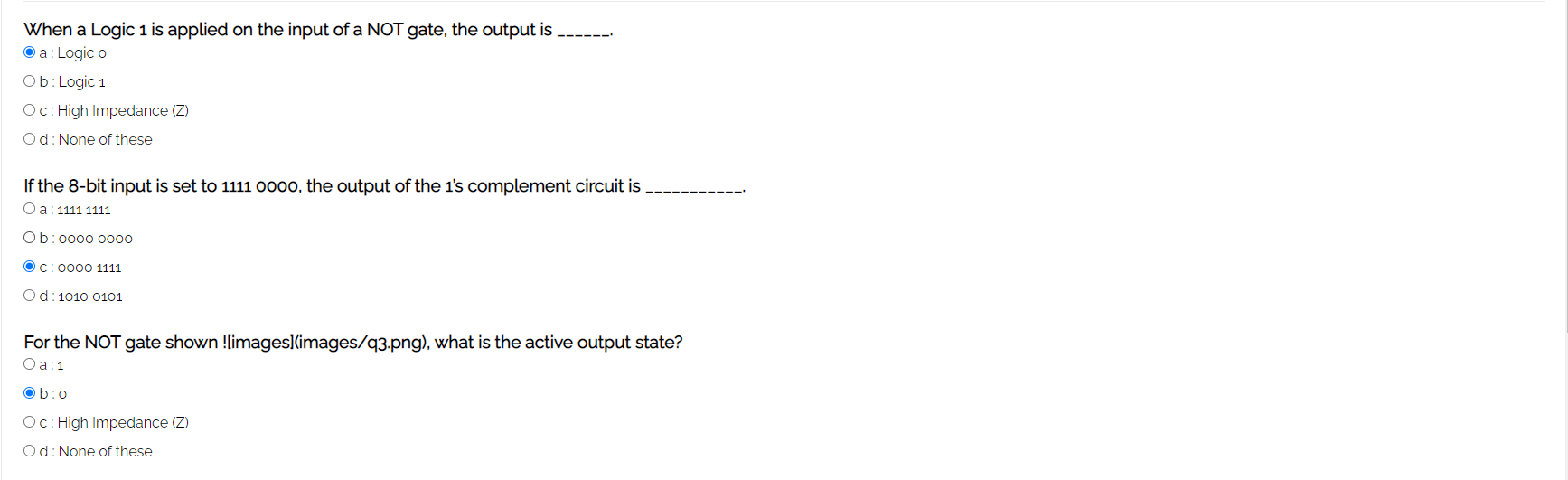
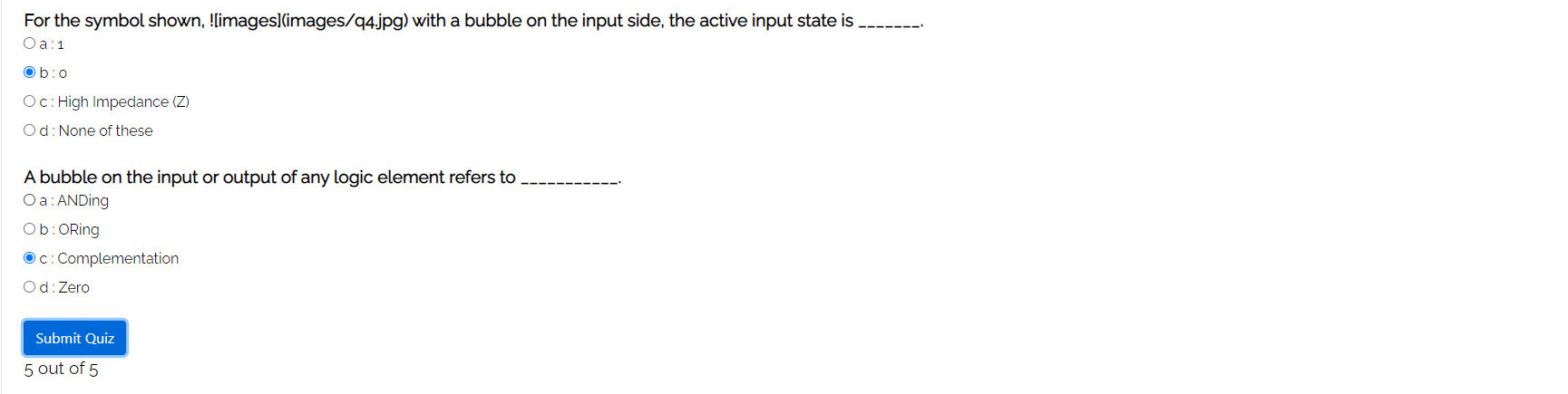
* **Pre-test :-**

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* **Simulation :-**

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* **Post-test :-**